Electric Power Systems Research 158 (2018) 37–44

Contents lists available at ScienceDirect

Electric Power Systems Research

journal homepage: www.elsevier.com/locate/epsr

A HVDC shunt tap based on unidirectional hybrid modular DC–DC converter with simultaneous charging and sequential discharging of capacitors

Ahmed A. Elserougi [a,b,*], Ahmed M. Massoud [a], Shehab Ahmed [c]

[a] Department of Electrical Engineering, Qatar University, Doha, Qatar
[b] Department of Electrical Engineering, Alexandria University, Alexandria, Egypt
[c] Department of Electrical and Computer Engineering, Texas A&M University at Qatar, Doha, Qatar

ARTICLE INFO

Article history:
Received 30 August 2017
Received in revised form
28 November 2017
Accepted 2 January 2018

Keywords:
Shunt tap
DC–DC converter
Hybrid modular converter

ABSTRACT

In this paper, a new HVDC shunt tap is proposed. The proposed configuration consists of a unidirectional hybrid modular DC–DC converter followed by a voltage source converter for DC–AC conversion to feed a local AC network connected to the tap output terminals. The proposed DC–DC converter consists of a high-voltage valve, and series-connected unidirectional half-bridge Sub-Modules (SMs). Unlike Marx generator circuit concept, the DC–DC conversion in the proposed configuration is achieved by enabling simultaneous charging of series-connected capacitors (i.e. SMs capacitors), and sequential discharging of capacitors. Compared to Marx-generator based switched capacitor DC–DC converters, the proposed configuration has a lower number of semiconductor devices, which affects positively the system cost, and reduces the control complexity. Detailed illustration, design, and control of the proposed approach are presented. Simulation results are presented to validate the proposed approach.

1. Introduction

In point-to-point HVDC systems, a small share of the total active power (less than 10% of the HVDC system power) can be tapped from the main HVDC circuit for local use of rural areas near to the HVDC transmission lines [1–5].

The cost of the employed tap should be kept low with a negligible impact on the main HVDC circuit in case of failure/fault in any of the tap components. Finally, the tap controller should not affect the main HVDC circuit controller [6].

Shunt and series taps can be employed for tapping a limited amount of power from the main HVDC circuit in point-to-point HVDC systems. Fig. 1 shows the basic operational concept of each tap assuming that the tap power is 10% of the transmitted power. Based on Fig. 1, it has to be noted that in the shunt tap, the input voltage to the shunt tap circuit is the DC voltage of the main HVDC circuit ($v_{tap} \sim= V_{dc}$), while its input current is low ($i_{tap} = 0.1 I_{dc}$). On the other hand, the input current of series tap is the DC current of the main HVDC circuit ($i_{tap} = I_{dc}$), while its input voltage is relatively low ($v_{tap} \sim= 0.1\ V_{dc}$). Based on that, the shunt tap should withstand the full DC voltage of the main HVDC circuit, which makes it more expensive compared with the series tap. However, shunt tap is more reliable. Different types of HVDC shunt tap have been proposed in literature. In Ref. [7], a recent review for different types of HVDC tap has been presented. The construction of main proposed taps in literature can be categorized into (i) a DC–AC converter followed by a step-down low frequency transformer [5,8–11], and (ii) a DC–DC converter followed by a low-voltage voltage source converter for DC–AC conversion [12,13].

With respect to the second category (which is the focus of this paper), different DC–DC converters have been employed such as DC–DC modular multi-level converter [12] and switched capacitor DC–DC converters [13]. The switched-capacitor DC–DC converter presented in Ref. [13] consists of a high-voltage valve and a number of series-connected Sub-Modules (SMs), where each SM consists of three Insulated Gate Bipolar Transistors (IGBTs) and a DC capacitor. The construction of the SM allows connecting the SMs capacitors in series or in parallel. The series/parallel connection of capacitors is used to apply Marx generator concept; where simultaneous charging of series-connected capacitors and simultaneous discharging of parallel-connected capacitors are employed in the switched DC–DC converter presented in Ref. [13].

* Corresponding author at: Department of Electrical Engineering, Qatar University, Doha, Qatar.
E-mail address: ahmed.elserogi@qu.edu.qa (A.A. Elserougi).

https://doi.org/10.1016/j.epsr.2018.01.004
0378-7796/

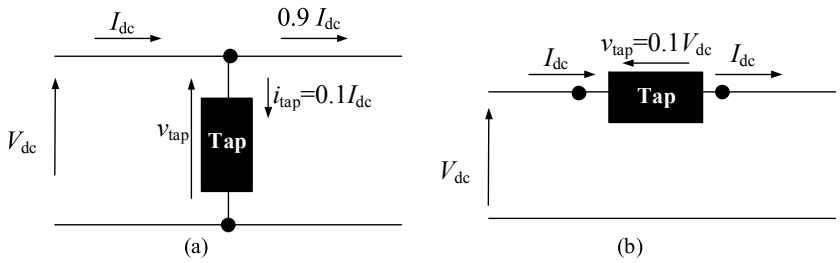

Fig. 1. Basic concept of shunt and series tap assuming tap power 10% of the sending end power (a) shunt tap, (b) series tap.

In this paper, the switched-capacitor DC–DC converter concept is employed, but with a different SM configuration, where a unidirectional half-bridge SM is employed. The unidirectional half-bridge SM consists of an IGBT, a diode, and a DC capacitor. In the proposed unidirectional hybrid modular DC–DC converter, simultaneous charging of series-connected capacitors, but sequential discharging of capacitors (one by one) are employed, instead of the simultaneous discharging of parallel-connected capacitors approach presented in Ref. [13]. The proposed configuration can achieve the desired DC–DC conversion with a lower count of semiconductor devices, which affects positively the system cost, and reduces control complexity.

A detailed illustration for the operational concept, design, and control of the proposed concept is presented. Finally, simulation results for the proposed concept are presented to validate the declared claims.

2. The proposed HVDC shunt tap

2.1. Architecture

The proposed HVDC shunt tap is shown in Fig. 2. The tap is connected across the main HVDC system to feed a medium voltage local AC network near to the HVDC transmission lines. The proposed configuration consists of a unidirectional hybrid modular DC–DC converter followed by a two-level voltage source converter for DC–AC conversion to feed the local AC network connected to the tap output terminals.

The proposed unidirectional hybrid modular DC–DC converter is responsible for stepping down the voltage from the DC voltage level of the main HVDC circuit (V_{dc}) to the desired DC voltage level (V_{dT}), meanwhile the power is transferred from the high-voltage side (V_{dc}) to the low-DC side (V_{dT}). While the two-level voltage source converter (VSC) is employed for DC–AC conversion to feed the local AC network.

The two-level VSC is operated to ensure pumping the desired active and reactive powers to the local AC network. Meanwhile, the DC-link voltage of the VSC is controlled to maintain it within a certain voltage level, i.e. DC-link voltage reference. The DC-link voltage controller estimates the amount of power to be pumped from the main HVDC circuit through the proposed hybrid modular DC–DC converter to keep the power balance.

In the following subsection, the operational concept of the proposed unidirectional DC–DC converter is presented to show how the power is transferred through the converter from a high-voltage side (V_{dc}) to a low voltage side (V_{dT}).

2.2. Operational concept of the unidirectional hybrid modular DC–DC converter

The proposed unidirectional hybrid modular DC–DC converter is called hybrid modular as it consists of a high-voltage valve (S_m), and unidirectional half-bridge SMs.

The high-voltage valve is implemented via series-connected IGBTs with proper static and dynamic voltage sharing. The number of employed SMs (n) depends on the ratio between the voltages of high-voltage side (V_{dc}) and low-voltage side (V_{dT}), where $n > (V_{dc}/V_{dT})$.

The proposed hybrid modular DC–DC converter has a unidirectional power transfer capability (from the high-voltage side to the low-voltage side), via turning on and off the valve (S_m) with a proper duty cycle (D). The duty cycle is controlled to ensure a certain amount of current (i_{tap}) is pumped from the main HVDC circuit into the tap. A smoothing inductance L_H is employed to ensure operating with a smoothed tap current (i_{tap}), i.e. the shunt tap is acting as a current source, as seen from the HVDC system, which facilitates a seamless shunt operation.

During turn-off period of the valve (S_m), the capacitors (C_1 to C_n) are connected in series, via turning-on the switches (S_1 to S_n) as shown in Fig. 3a. As a result, series-connected capacitors are charged and the inductor discharges. The total voltage across the series-connected capacitors will be higher than the DC voltage of the main HVDC circuit (V_{dc}) due to the boosting action of high-voltage valve switching with the existence of the inductance L_H. The voltage of each capacitor equals the total voltage across the series-connected capacitors divided by their number (n).

The voltage of each capacitor is slightly higher than the DC-link voltage of the VSC, so if the capacitors "C_1 to C_n" are connected sequentially across the DC terminal of VSC, the energy stored in capacitors will be pumped into the VSC DC-link. The sequential discharging of capacitors "C_1 to C_n" is presented as follows.

During the turn-on period of the valve (S_m), the inductor L_H charges. Meanwhile the capacitors are connected sequentially (one by one) across the DC-link of the two-level VSC as shown in Fig. 3b–d via turning-on the switches (S_1 to S_n) sequentially (sequential discharging of capacitors "C_1 to C_n"). The turn-on duration of valve S_m, which is DT_s (where T_s is switching period), is divided equally between the SMs, i.e. each SM is connected to the DC-link of the two-level VSC for time duration of DT_s/n.

It has to be noted that to avoid inrush current due to parallel connection of capacitors during the sequential discharging period (Fig. 3b–d), a limiting resistance (r_{limit}) is employed. The limiting resistance is selected to ensure a limited current and insignificant power losses through it.

The aforementioned sequence can be executed by keeping the switching pattern of switches shown in Fig. 4. The corresponding variation of system variables with the switching is also shown in Fig. 4.

The inductor current increases during the turn-on period of the valve S_m, while it decreases during the turn-off period of the valve S_m. The inductance (L_H) should be selected properly to ensure a low-ripple input current from the main HVDC circuit (i_{tap}). On the other hand, the capacitors "C_1 to C_n" are discharged sequentially during the turn-on period of valve S_m, while they are charged simultaneously during turn-off time of the valve (S_m) due to connecting them in series. It has to be noted that during the discharging of capac-

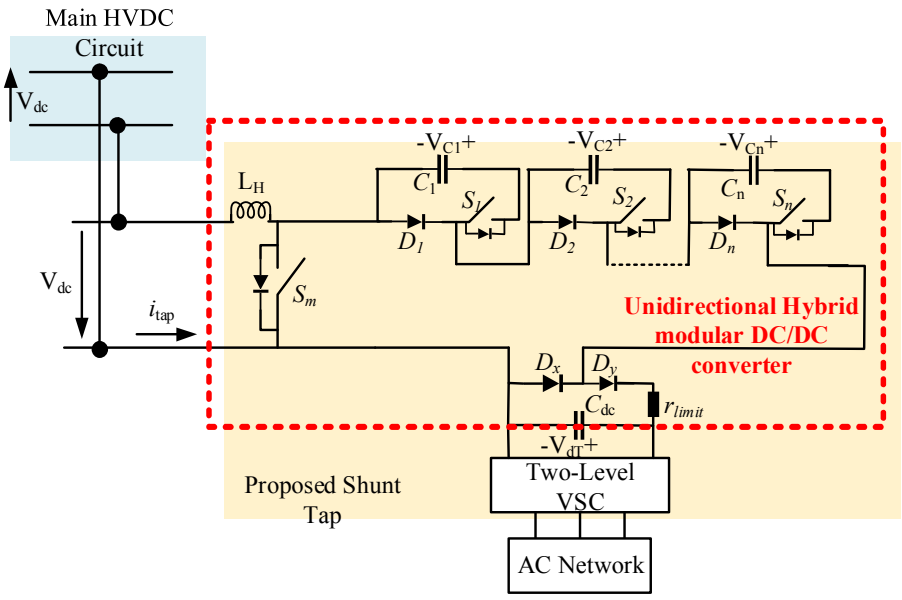

Fig. 2. The proposed HVDC shunt tap.

itors "C_1 to C_n", the voltage of two-level VSC DC-link capacitance (V_{dT}) increases, as the capacitors "C_1 to C_n" discharge their energy sequentially in it. While during the charging of capacitors "C_1–C_n", the voltage of two-level VSC DC-link capacitance decreases due to pumping its energy to the local AC network through the two-level VSC.

To ensure a successful operation, the proposed converter should be operated with a proper duty cycle (D) to ensure the power balance condition. This can be done by estimating the proper operational duty cycle with the help of DC-voltage controller at the DC terminals of the VSC as illustrated in the following section.

3. IGBTs switching losses

In this part, the switching losses of the involved IGBTs in the proposed unidirectional hybrid modular DC–DC converter are presented. Based on Figs. 3 and 4, the switching losses of high-voltage valve (S_m) are given by;

$$P_{swSm} \cong 0.5\frac{V_{dc}}{(1-D)}\left(i_{tap} + P_{VSC}/DV_{dT}\right) f_s \left(t_{on} + t_{off}\right) \quad (1)$$

where f_s is the switching frequency of the high-voltage valve S_m, t_{on} and t_{off} are its turn-on and turn-off times, P_{VSC} is the average active power drawn from the VSC DC-link, D is the duty cycle of the high-voltage valve S_m, and V_{dT} is the DC-link voltage of the VSC.

On the other hand, the switching losses of IGBTs in the unidirectional half-bridge SMs (P_{swHB}) is given by;

$$P_{sw\ HB} \cong 0.5V_C\,(n-1)\left(i_{tap} + \left(P_{VSC}/DV_{dT}\right)\right) f_s \left(t_{on} + t_{off}\right) \quad (2)$$

where V_C is the capacitor voltage, and t_{on} and t_{off} are the turn-on and turn-off times of the involved IGBTs in SMs.

4. Closed loop control of the proposed configuration

Fig. 5 shows the closed loop controller for the proposed HVDC shunt tap, which consists of two parts, the VSC active and reactive power controller (Fig. 5a) and the controller of the hybrid modular DC–DC converter (Fig. 5b). With respect to the active and reactive power control of VSC, different methods can be employed to ensure pumping the desired active and reactive powers into the local AC network such as dq-reference frame-based active and reactive power control in Ref. [14], and the power angle control in Refs. [15,16]. This part is out of the paper's scope where any conventional technique can be employed to generate the reference three-phase voltages of the VSC. Then the VSC modulating signals can be estimated simply by dividing the extracted reference three-phase voltages by $0.5\,V_{dT}$. Finally, the gate pulses of VSC can be generated by comparing the extracted modulating signals with a proper carrier. It has to be noted that power angle control is applied in the presented work to ensure pumping the desired active and reactive power to the local AC network.

As the two-level VSC is pumping the desired active power to the local AC network, the DC-link capacitor decreases. To replenish the DC-link voltage, a proper amount of power should be drawn from the main HVDC link circuit. This can be done by employing a PID-based DC-voltage controller on the V_{dT} voltage as shown in Fig. 5b, to estimate the amount of power (P_{ref}) to be pumped from the main HVDC circuit into the VSC DC-link capacitance through the hybrid modular DC–DC converter. The power reference (P_{ref}) is given by;

$$P_{ref} = (V_{dT\,ref} - V_{dT})G_1(s) \quad (3)$$

where $G_1(s)$ is the transfer function of the first PID controller (voltage controller). Then the power reference (P_{ref}) is divided by (V_{dc}) to estimate the reference DC current to be drawn by the tap (i_{ref}). The difference between the extracted reference and actual currents is fed to a PID controller to extract the suitable duty cycle. The extracted duty cycle is given by;

$$D = (i_{ref} - i_{tap})G_2(s) \quad (4)$$

where $G_2(s)$ is the transfer function of the second PID controller (current controller). Finally, with the help of the extracted duty cycle and switching period (T_s), the gate pulses of the involved switches in the hybrid modular DC–DC converter can be generated with the same pattern shown in Fig. 4 to ensure sequential discharging and simultaneous charging of capacitors "C_1 to C_n" with the operation.

5. Design of the proposed configuration components

In this section, the design of high voltage inductor (L_H), SM capacitors, VSC DC-link capacitance, and limiting resistance are presented.

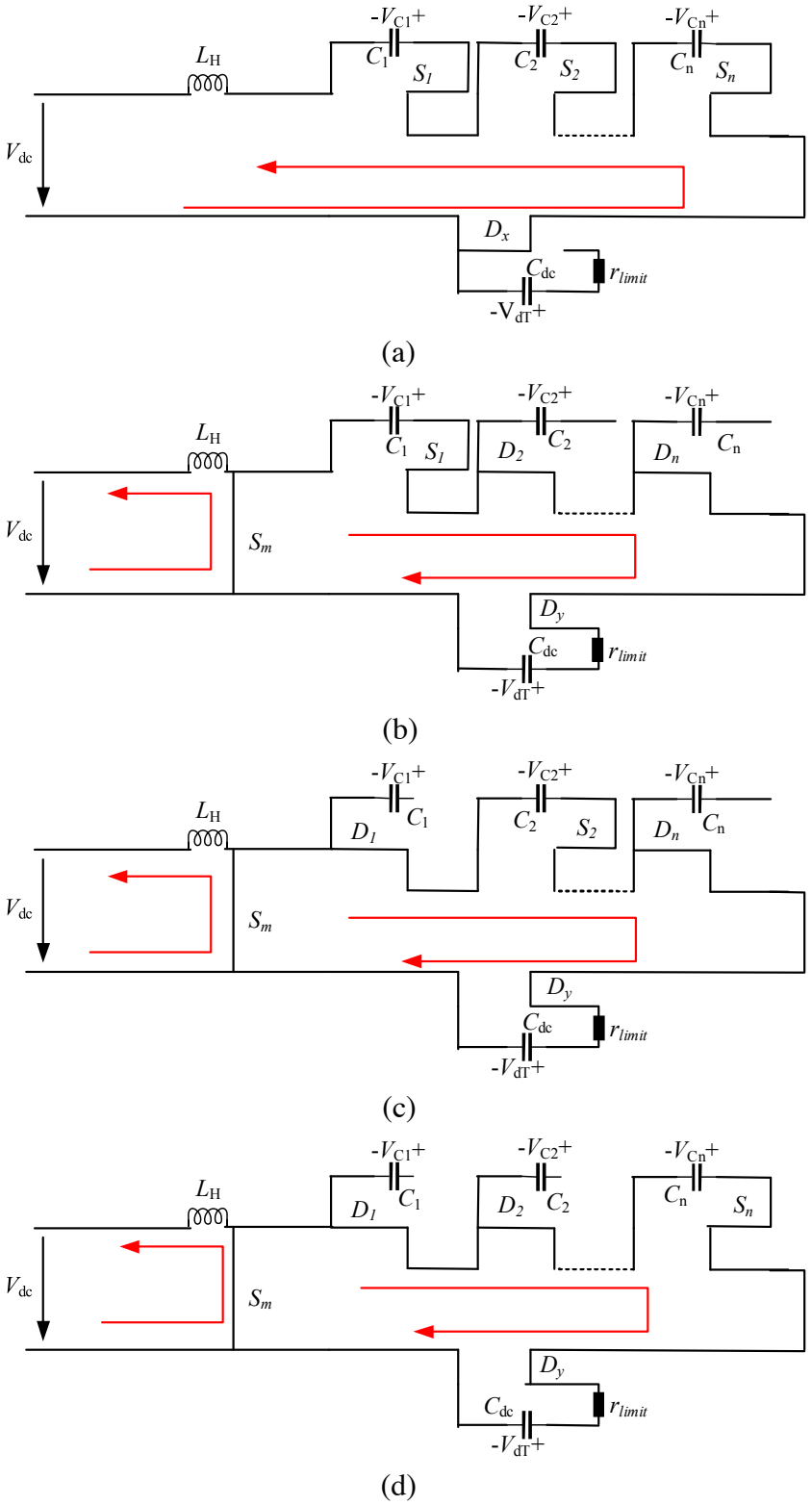

Fig. 3. Operational modes of the proposed unidirectional hybrid modular DC–DC converter (a) charging of series-connected capacitors "C_1–C_n", (b)–(d) sequential discharging of capacitors "C_1–C_n".

5.1. High-voltage inductor

The inductance (L_H) should be selected to ensure a certain ripple content (Δi_{tap}) in the input current of the tap (i_{tap}). During the turn-on period of the valve (S_m), the relation between the inductance value and change in the current can be expressed by,

$$V_{dc} = L_H \frac{\Delta i_{tap}}{DT_s} \tag{5}$$

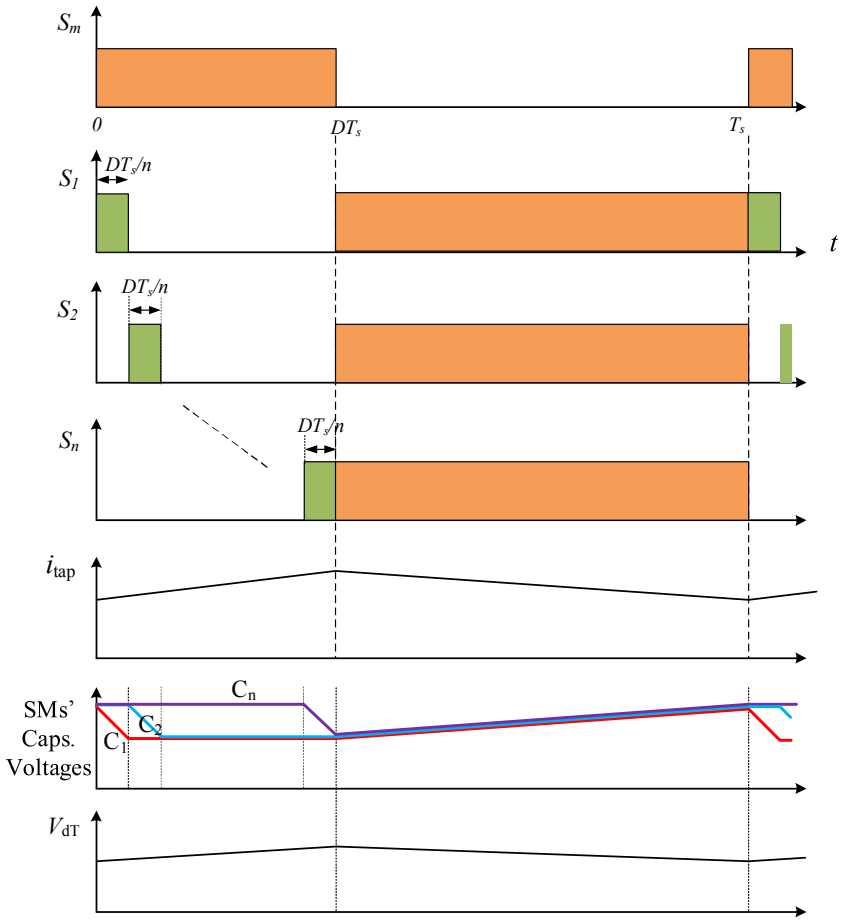

Fig. 4. Switching pattern of the involved switches along with variation of system variables with the switching.

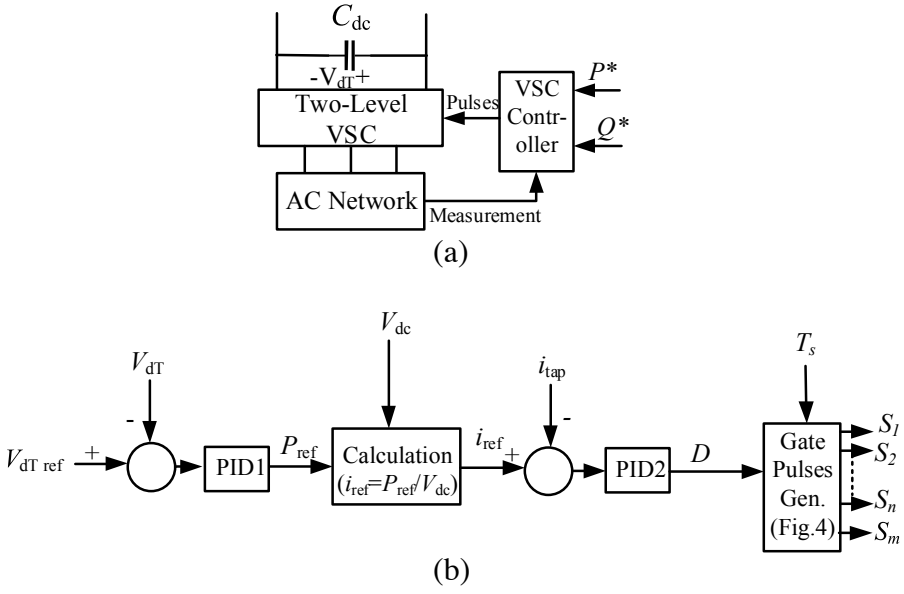

Fig. 5. Closed loop control of the proposed configuration. (a) active and reactive power control of VSC and (b) control of the hybrid modular DC–DC converter.

i.e.,

$$L_H = V_{dc}\frac{DT_s}{\Delta i_{tap}} \tag{6}$$

Based on Eq. (6), for desired peak-to-peak ripple current, suitable inductance can be selected. To ensure transferring of power from high-voltage side into the low-voltage side, the duty cycle of the high-voltage valve should fulfil the following condition,

$$D > 1 - \left(\frac{V_{dc}}{nV_{dT}}\right) \tag{7}$$

The critical value of duty cycle can be used in component selection.

5.2. Submodules' capacitors

During the turn-off period of high-voltage valve (S_m), the SMs capacitors (C_i) are connected in series to be charged. The capacitance (C_i) can be selected to ensure a certain voltage ripple content (Δv_c). The relation between the capacitance value and its voltage change can be expressed by,

$$i_{tap} = C_i \frac{\Delta v_c}{T_s (1 - D)} \tag{8}$$

i.e.

$$C_i = i_{tap} \frac{T_s (1 - D)}{\Delta v_c} \tag{9}$$

Based on the desired peak-to-peak voltage ripple (Δv_c), the suitable SM capacitance can be selected.

5.3. DC-link capacitance of two-level VSC

The DC capacitor size is characterized as a time constant, which equals the ratio between the total energy stored energy in it at the rated voltage to the converter nominal apparent power, i.e.

$$\tau = \frac{\frac{1}{2} C_{dc} V_{dT}^2}{S_{VSC}} \tag{10}$$

The time constant is the time needed to charge the capacitance C_{dc} from zero to V_{dT} when the converter is supplied with a constant active power of S_{VSC} [17].

To limit the capacitors inrush current peak and to maintain almost constant current level during sequential connection period, a high time constant is required.

5.4. Limiting resistance

The limiting resistance is employed to limit the capacitors inrush currents during the sequential connection. The power dissipated in the limiting resistance should be insignificant to ensure efficient operation. Eq. (11) gives the expression for the power dissipated in the limiting resistance; assuming that the capacitances are high enough to assume almost constant current (I_x) passes through them during the sequential connection.

$$P_{R_i} = D I_x^2 R_i \tag{11}$$

Based on the power invariance condition, the current level I_x is given by,

$$I_x = \frac{V_{dc} i_{tap}}{D V_{dT}} \tag{12}$$

i.e. the limiting resistance is given by,

$$R_i = \frac{\alpha P_{VSC} D V_{dT}^2}{\left(V_{dc} i_{tap}\right)^2} \tag{13}$$

where α is the ratio between the dissipated power in R_i to the active power of VSC load, P_{VSC} is the active power of the VSC load.

6. Simulation

A simulation model has been built for the proposed shunt tap (Fig. 2) along with the proposed closed loop controller (Fig. 5b) to investigate its performance during different active and reactive power levels pumped to the local AC network. The simulation parameters are given in Table 1. The parameters are selected based on the aforementioned equation to satisfy the desired specifications ($\Delta i_{tap} < 20$ A, $\Delta v_c < 40$ V, time constant $\tau = 180$ ms, and $\alpha = 0.005$).

Table 1
Simulation parameters.

Parameter	Value
Voltage of high-voltage side, V_{dc}	25 kV
Reference voltage of VSC DC-link, V^*_{dT}	10 kV
Number of submodules, n	3
Submodule capacitance	2 mF (pre-charged voltage = 10 kV)
VSC DC-link capacitance	10 mF (pre-charged voltage = 10 kV)
Switching periodic time of the valve (S_m), T_s	1 ms
VSC switching frequency	5 kHz
Smoothing inductor, L_H	0.25 H
Limiting resistance, r_{limit}	0.04Ω
Local AC network	Three-phase constant impedance load 9.4 + j9.4 Ω
Modulating signals peak of VSC	Step changes from 1 to 0.707 at $t = 3$ s
PID1 transfer function, $G_1(s)$	$1 \times 10^4 + \frac{4 \times 10^4}{s} + \left(\frac{1 \times 10^5}{1 + \frac{100}{s}}\right)$
PID2 transfer function, $G_2(s)$	$1 \times 10^{-4} + \frac{1 \times 10^{-3}}{s}$

In the presented case, the active and reactive powers are reduced from 2 MW/2 MVAR to 1 MW/1 MVAR at $t = 3$, the corresponding simulation results are shown in Fig. 6 assuming that the SMs' capacitors as well as VSC DC-link capacitor are pre-charged with 10 kV. Fig. 6a shows the voltage of VSC DC-link (V_{dT}), where the voltage is kept constant at 10 kV with the operation, which guarantees the power balance between the power pumped to the local AC network, and the power pumped from the main HVDC circuit to the VSC DC-link through the hybrid modular DC–DC converter. Fig. 6b shows the voltages of capacitors "C_1 to C_n", where the voltages are slightly higher than V_{dT}, i.e. the power is pumped from the high-voltage side to the low-voltage side. The zoomed-in view of variation of capacitors voltages with the operation is shown in Fig. 6c where the capacitors are discharged sequentially (one by one) and charged simultaneously. It is clear that (i) the peak-to-peak ripple voltage is as desired (i.e. less than 40 V), and (ii) there is a voltage difference between the voltages of SMs' capacitors, this is due to the increasing of DC-link voltage (V_{dT}) during the sequential discharging period.

Fig. 6d shows the power reference (P_{ref}) extracted from the DC-voltage controller at the DC terminals of the VSC. It is clear that the extracted reference power changes with the variation of the power pumped to the local AC network fed by the VSC, i.e. power balance is achieved.

Fig. 6e shows the corresponding input tap current (i_{tap}), where the current is a continuous DC current with a low ripple content (less than 20 A, as defined in the specifications). Fig. 6f shows the duty cycle (D) of valve S_m which is extracted from the tap current controller. Fig. 6g and h show the current passing through the limiting resistance (r_{limit}), while the input current of VSC at its DC terminals is shown in Fig. 6i and j, where the current is discontinuous and its peak equals the load current peak.

The generated phase currents at the AC side of VSC are shown in Fig. 6k. Finally, the active and reactive power pumped to the local AC network fed by the VSC are shown in Fig. 6l (the reactive power pumped to the AC network has the same profile of the active power as a load with 0.707 lagging power factor is employed).

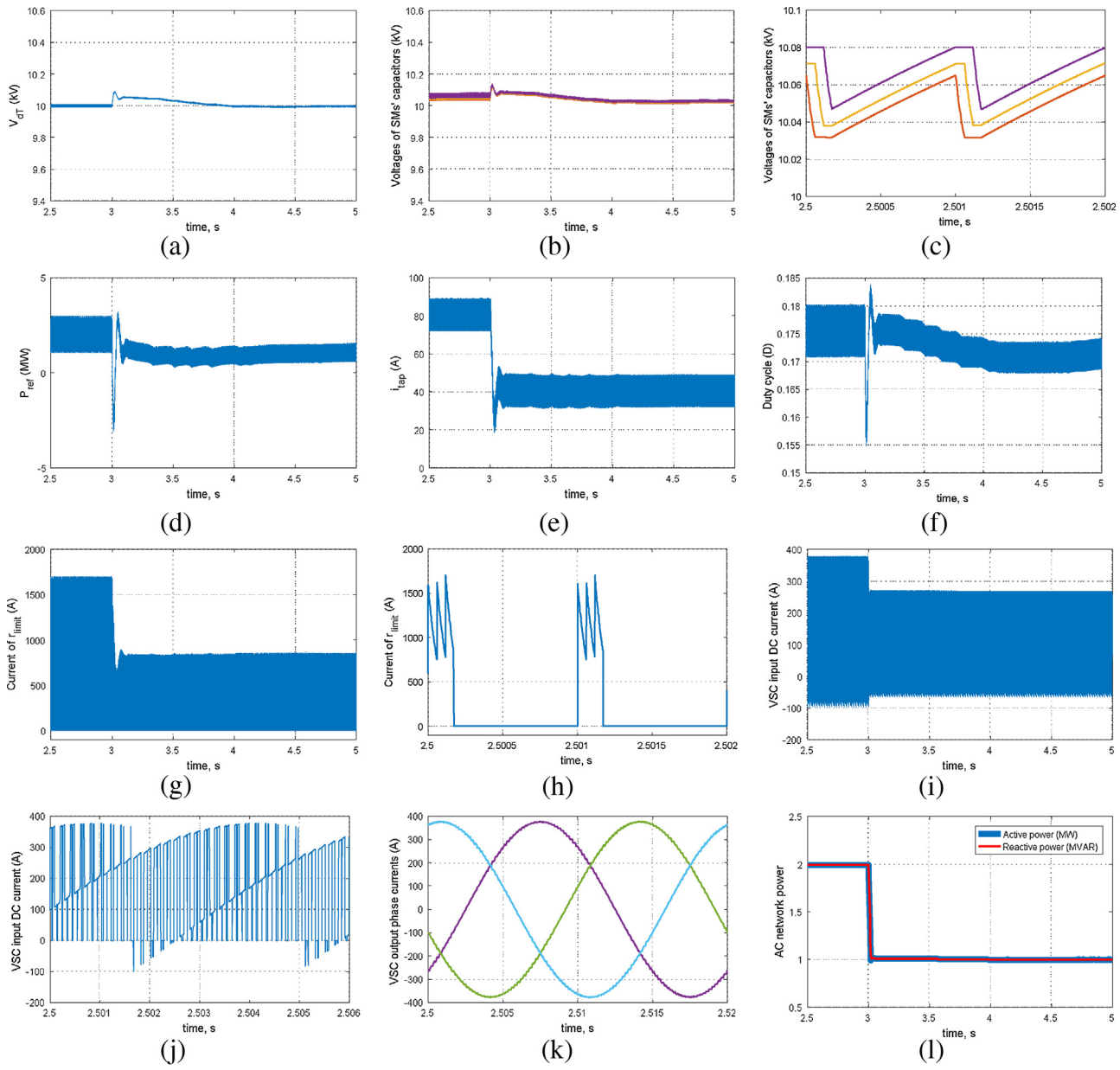

Fig. 6. Simulation results. (a) DC-link voltage of VSC, (b) voltages of SMs' capacitors, (c) zoomed-in version of voltages of SMs' capacitors, (d) reference power to be drawn from the main HVDC circuit, (e) input DC current to the shunt tap, (f) duty cycle of the valve S_m, (g) current passes through the limiting resistance, (h) zoomed-in view for the current passes through limiting resistance, (i) VSC input DC current, (j) zoomed-in view of the VSC input current, (k) VSC output phase currents, and (l) active and reactive power pumped to the local AC network fed by the VSC.

7. Conclusion

In this paper, a transformer-less HVDC shunt tap is proposed. The proposed tap consists of a unidirectional hybrid modular DC–DC converter followed by a two-level VSC. The proposed hybrid modular DC–DC converter provides a DC–DC conversion with a lower count of semiconductor devices compared to the Marx-generator switched capacitor DC–DC converters, where simultaneous charging and sequential discharging of capacitors are employed with the help of a unidirectional half-bridge SMs. The proposed hybrid modular DC–DC converter is responsible for stepping down the voltage and injecting the power from the high-voltage side to the low-voltage side, while the VSC is responsible for DC–AC conversion to feed the local AC network connected to the tap output terminals. In the presented work, the VSC is operated to ensure pumping the required active and reactive powers to the local AC network connected to it, where the VSC is absorbing the required energy from its DC-link capacitance. To replenish the DC-link capacitance of VSC, a certain amount of power should be pumped from the main HVDC circuit into the VSC DC-link through the hybrid modular DC–DC converter. To achieve that, DC-voltage controller at the VSC DC-link is employed to determine the power level to be absorbed from the main HVDC circuit. The input tap current is controlled to ensure drawing this amount of power. The current control determines the proper duty cycle of the involved high-voltage valve. A detailed illustration of operational concept, closed loop control, and design of the proposed configuration are presented. Finally, simulation results are presented to validate the proposed configuration.

Acknowledgement

This publication was made possible by NPRP grant NPRP (9-092-2-045) from the Qatar National Research Fund (a member of Qatar Foundation). The statements made herein are solely the responsibility of the authors.

References

[1] M. Bahrmam, M. Baker, J. Bowles, R. Bunch, J. Lemay, W. Long, J. McConnach, R. Menzies, J. Reeve, M. Szechtman, Integration of small taps into (existing) HVDC links, IEEE Trans. Power Deliv. 10 (1995) 1699–1706.
[2] D. Jovcic, B.T. Ooi, Tapping on HVDC lines using DC transformers, Electr. Power Syst. Res. 81 (2011) 561–569.
[3] A. Ekstrom, P. Lamell, HVDC tapping station: power tapping from a DC transmission line to a local AC network, International Conference on AC and DC Power Transmission (1991) 126–131.
[4] M. Aredes, C. Portela, F.C. Machado, A 25-MW soft-switching HVDC tap for ±500-kV transmission lines, IEEE Trans. Power Deliv. 19 (2004) 1835–1842.
[5] G. Asplund, A. Williamson, A novel approach to providing on route power supplies to rural and urban communities in close proximity to the extra high voltage DC transmission line, Power Engineering Society Conference and Exposition in Africa, 2007. Power Africa '07. IEEE (2007) 1–6.
[6] M.R. Aghaebrahimi, R.W. Menzies, Small power tapping from HVDC transmission systems: a novel approach, IEEE Trans. Power Deliv. 12 (October (4)) (1997) 1698–1703.
[7] Abdelrahman Ismail, M.S. Hamad, Amr El Zawawi, Emtethal Negm Abdallah, A review of recent HVDC tapping topologies, Eighteenth International Middle East Power Systems Conference (MEPCON) (2016).
[8] Quanrui Hao, Boon-Teck Ooi, Tap for classical HVDC based on multilevel current-source inverters, IEEE Trans. Power Deliv. 25 (4) (2010) 2626–2632.
[9] Z. Zhao, M.R. Iravani, Application of GTO voltage-source inverter for tapping HVDC power, IEE Proc. Gener. Transm. Distrib. 141 (1) (1994) 19–26.
[10] Ahmed Elserougi, Ahmed M. Massoud, Ayman S. Abdel-Khalik, Shehab Ahmed, A grid-connected HVDC shunt tap based on series-input parallel-output DC–AC multi-module 2-level voltage source converters, IEEE 8th GCC Conference & Exhibition (2015) 1–5.
[11] Ahmed Elserougi, Ahmed Massoud, Ayman Abdel-Khalik, S. Ahmed, HVDC shunt tap based on series-input parallel-output DC–AC multi-module VSCs with DC voltages balancing, 7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014) (2014) 1–6.
[12] T. Lüth, M.M.C. Merlin, T.C. Green, Modular multilevel DC/DC converter architectures for HVDC taps, in: 16th European Conference on Power Electronics and Applications, (EPE'14-ECCE Europe), August, 2014, pp. 1–10.
[13] J. Maneiro, S. Tennakoon, C. Barker, Scalable shunt connected HVDC tap using the DC transformer concept, in: 16th European Conference on Power Electronics and Applications, (EPE'14-ECCE Europe), August, 2014, pp. 1–10.
[14] M.P. Kazmierkowski, L. Malesani, Current control techniques for three-phase voltage-source PWM converters: a survey, IEEE Trans. Ind. Electron. 45 (October (5)) (1998) 691–703.
[15] J. Svensson, Grid-Connected Voltage Source Converter, Ph.D. Dissertation, Chalmers Univ. Technol., Gothenburg, Sweden, 1998.
[16] J. Svensson, Simulation of power angle controlled voltage source converter using a linear quadratic method in a wind energy application, 5th IEEE Workshop on Computers in Power Electronics (1996) 157–162.
[17] Cuiqing Du, The Control of VSC-HVDC and its Use for Large Industrial Power Systems, Thesis, Department of Electric Power Engineering, Chalmers University of Technology, Sweden, 2003.